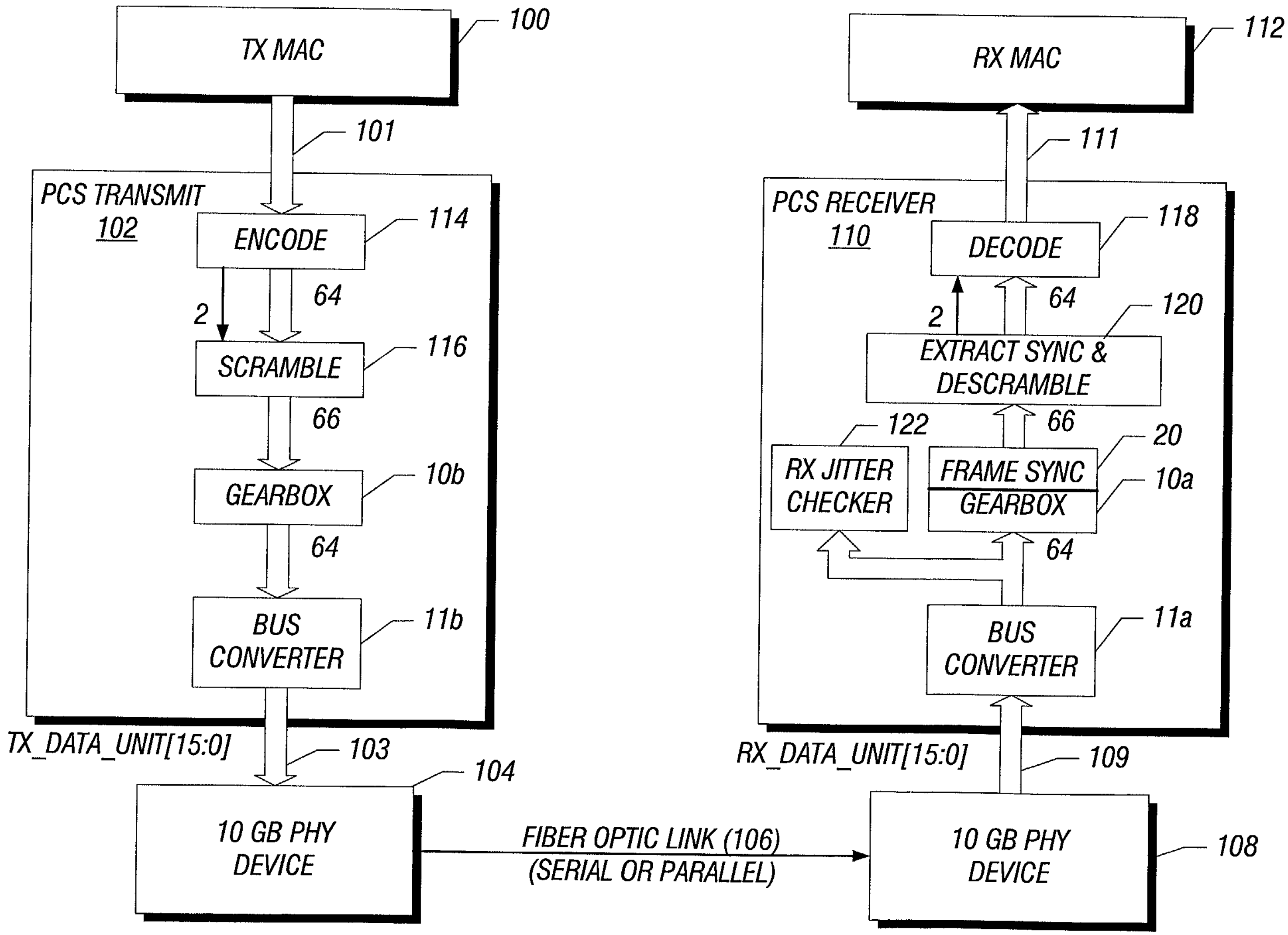
TX MAC
100
101
PCS TRANSMIT
102
ENCODE
114
2
64
SCRAMBLE
116
66
GEARBOX
10b
64
BUS CONVERTER
11b
TX_DATA_UNIT[15:0]
103
104
10 GB PHY DEVICE
FIBER OPTIC LINK (106)
(SERIAL OR PARALLEL)
RX MAC
112
111
PCS RECEIVER
110
DECODE
118
2
64
EXTRACT SYNC & DESCRAMBLE
120
122
66
20
RX JITTER CHECKER
FRAME SYNC
GEARBOX
10a
64
BUS CONVERTER
11a
RX_DATA_UNIT[15:0]
109
10 GB PHY DEVICE
108

FIG. 1

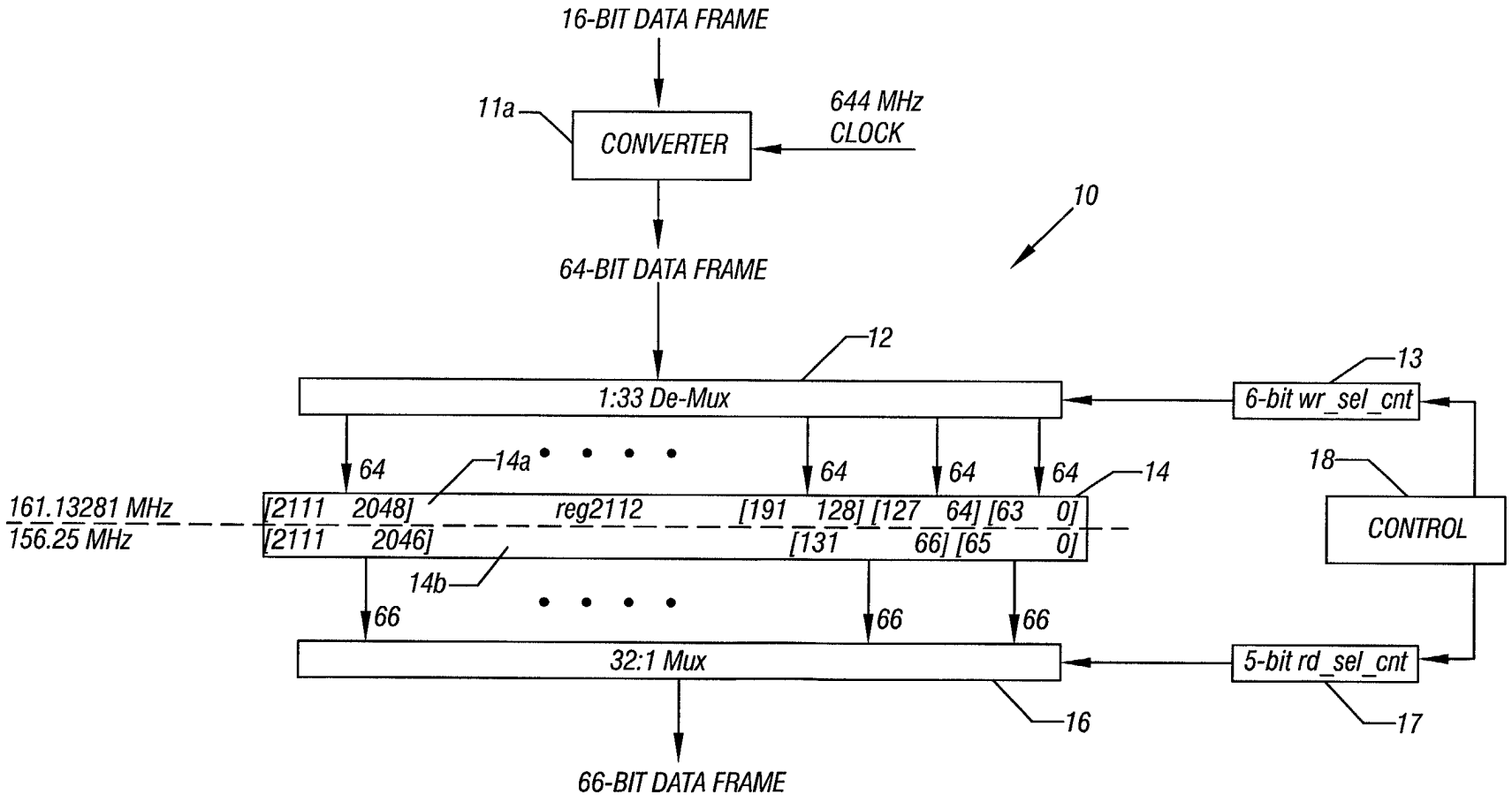
16-BIT DATA FRAME
11a
CONVERTER
644 MHz
CLOCK
10
64-BIT DATA FRAME
12
1:33 De-Mux
13
6-bit wr_sel_cnt
64
14a
64
64
64
14
18
161.13281 MHz
156.25 MHz
[2111 2048]
reg2112
[191 128] [127 64] [63 0]
[2111 2046]
[131 66] [65 0]
CONTROL
14b
66
66
66
32:1 Mux
5-bit rd_sel_cnt
16
17
66-BIT DATA FRAME

FIG. 2

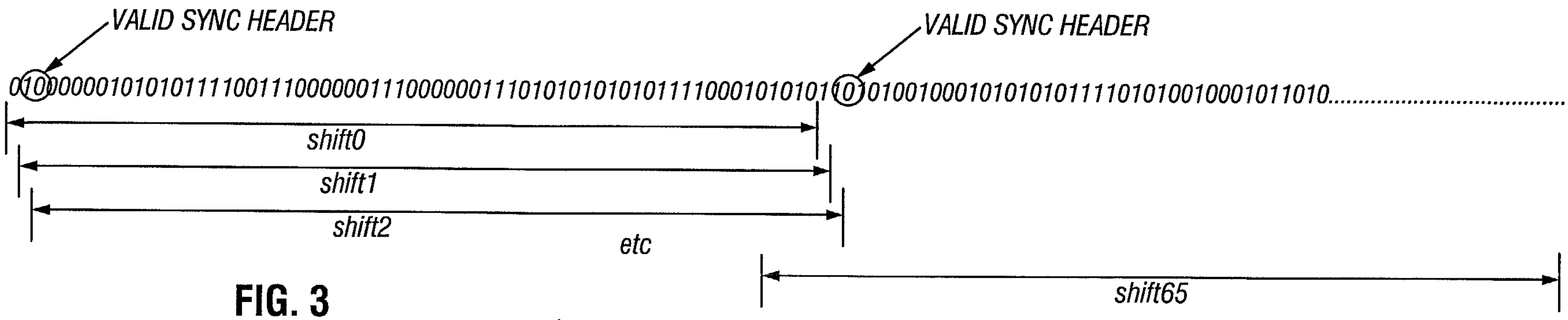
VALID SYNC HEADER
VALID SYNC HEADER
0100000001010101111001110000000111000000011101010101010111100010101011001001000101010101111010100100010110 10......................................
shift0
shift1
shift2
etc
shift65

FIG. 3

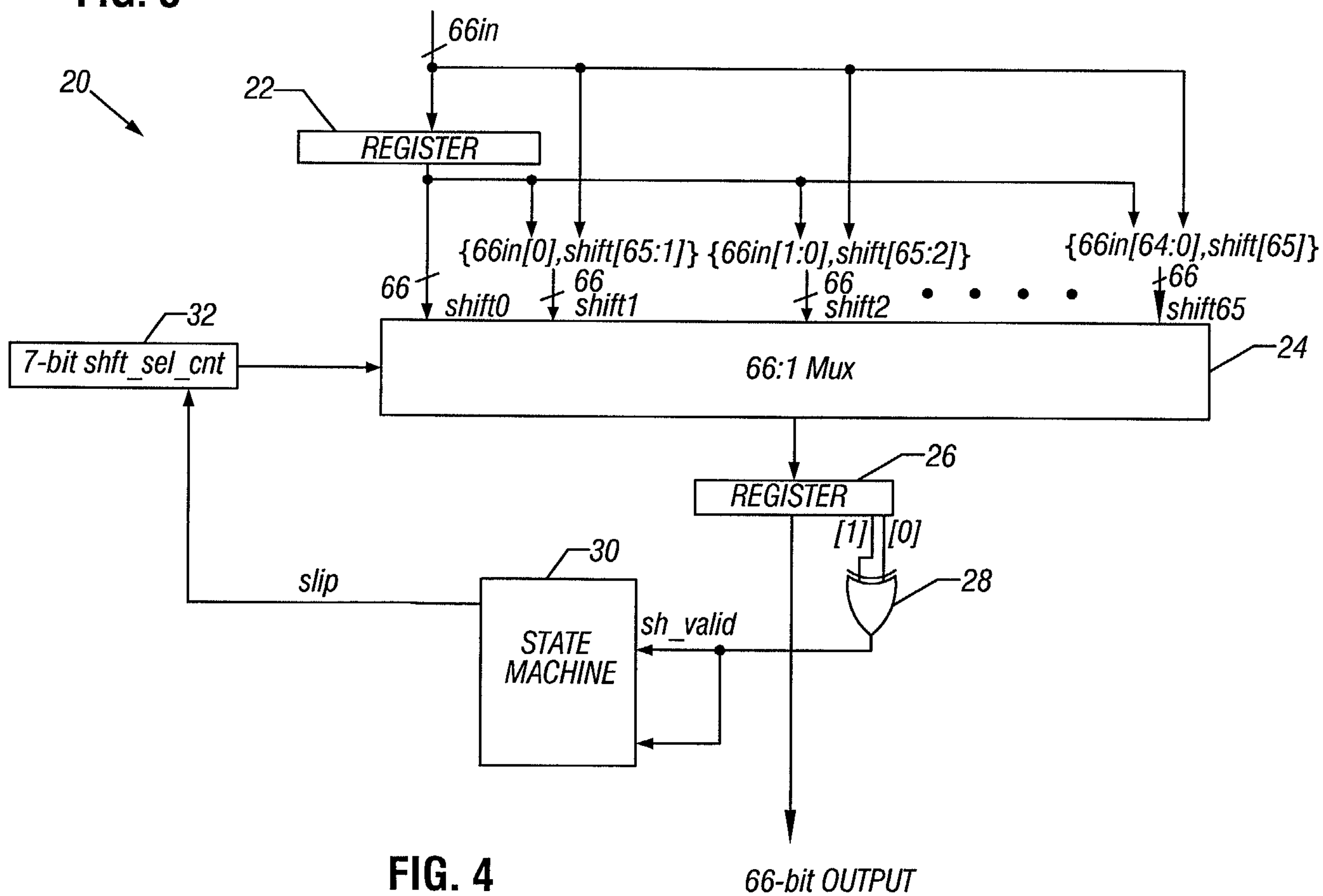
20
66in
22
REGISTER
{66in[0],shift[65:1]}
{66in[1:0],shift[65:2]}
{66in[64:0],shift[65]}
66
shift0
66
shift1
66
shift2
66
shift65
32
7-bit shft_sel_cnt
66:1 Mux
24
26
REGISTER
[1]
[0]
28
30
slip
STATE MACHINE
sh_valid
66-bit OUTPUT

FIG. 4

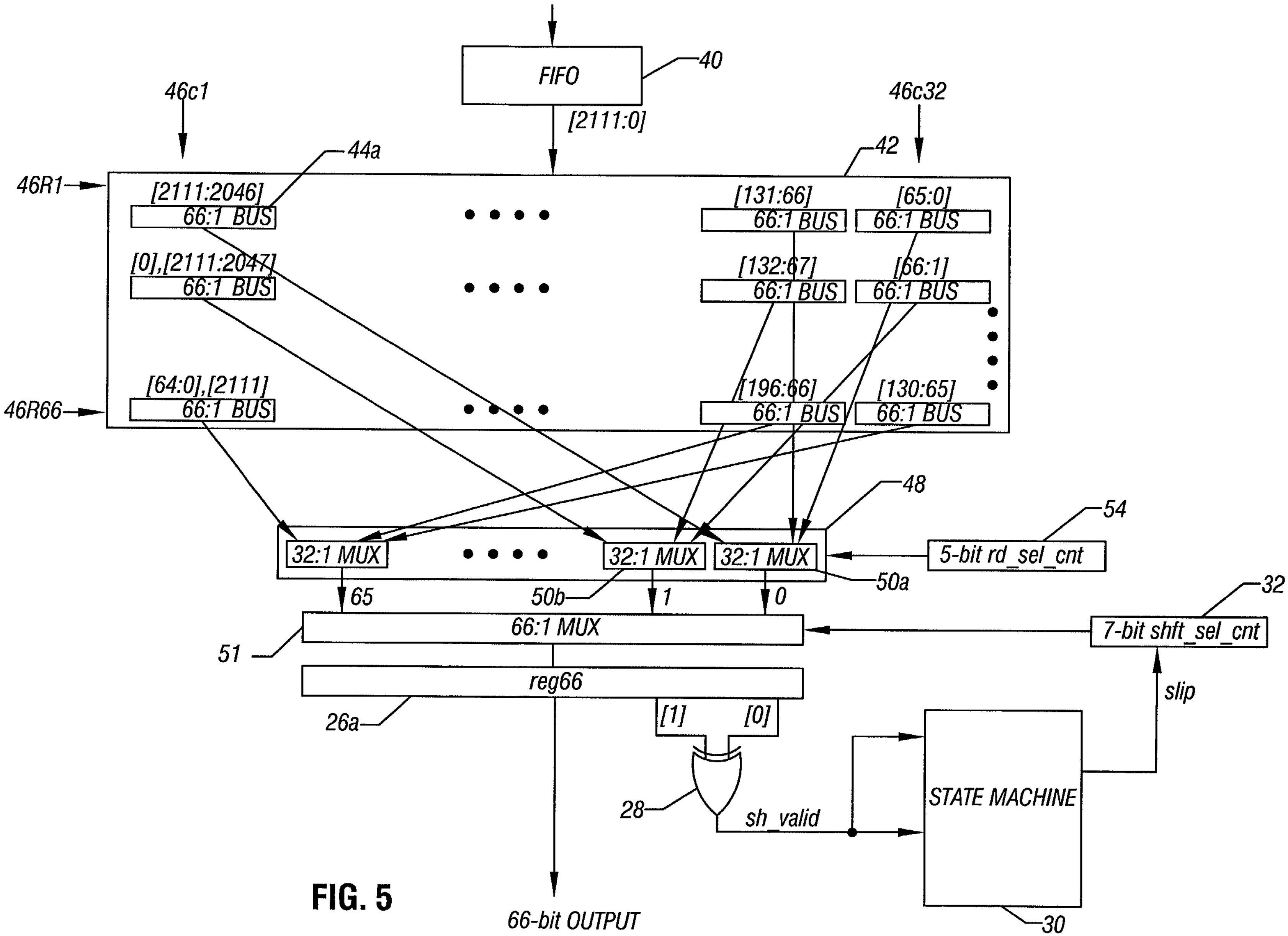
FIFO
40
[2111:0]
46c1
46c32
42
44a
46R1
46R66
[2111:2046]
66:1 BUS
[0],[2111:2047]
66:1 BUS
[64:0],[2111]
66:1 BUS
[131:66]
66:1 BUS
[65:0]
66:1 BUS
[132:67]
66:1 BUS
[66:1]
66:1 BUS
[196:66]
66:1 BUS
[130:65]
66:1 BUS
48
54
32:1 MUX
32:1 MUX
32:1 MUX
5-bit rd_sel_cnt
50a
50b
65
1
0
32
66:1 MUX
7-bit shft_sel_cnt
51
reg66
26a
[1]
[0]
slip
28
sh_valid
STATE MACHINE
30
66-bit OUTPUT

FIG. 5

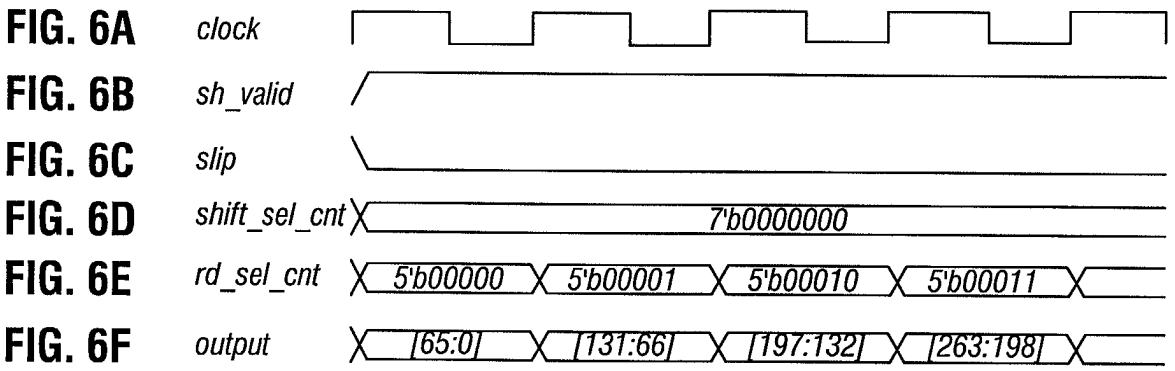

FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

FIG. 6F

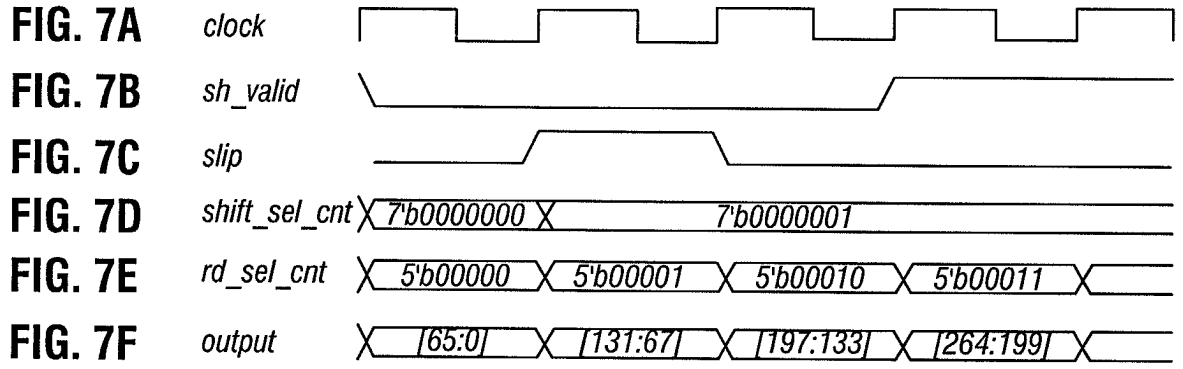

FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

FIG. 7E

FIG. 7F